

Thesis
B.Sc.

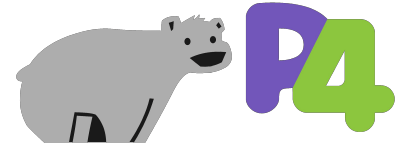
Thesis
M.Sc.

IDP

Event processing in Software Data Planes

Motivation

P4 is a programming language that describes the behavior of packet processing systems. P4 was introduced in 2014 and can be used to define entirely new networks with new protocols which behave differently from the networks we currently use. Compilers exist for various targets (software, FPGA, SmartNIC, ASIC).



P4 programming language

One of the existing P4 software targets is `t4p4s` which is built on top of DPDK. The Dataplane Development Kit (DPDK) is an open-source collection of libraries and drivers for high-performant packet processing. It runs in the userspace.

Some while ago, a P4 event architecture was presented for the SUME architecture on the NetFPGA. We reimplemented a similar architecture in the software target `t4p4s`. There, two pulling-based queues are processed in every iteration. DPDK timers are used to trigger timing-based events.

This thesis aims to define different parameters' influences on performance experimentally. This includes the update frequency of the timers, the cost of creating events, and the cost of checking for new events regularly. Another interesting investigation is the interference of regular packets and events in different traffic/event patterns. Based on the findings, the current implementation can also be improved or extended, e.g., by replacing the mechanism through DPDK-based events.

Tasks

The thesis requires diving into *DPDK*, and *t4p4s*:

- Get familiar with involved technologies and programs
- Systematically evaluate the performance parameters of the event architecture
- Extend/optimize the implementation

Requirements

- Experience with C/C++ programming is recommended
- Experience with Linux is required

Sources

- <https://p4.org/>
- <https://github.com/P4ELTE/t4p4s>
- S. Ibanez et al., Event-Driven Packet Processing, 2019, HotNets '19, <https://doi.org/10.1145/3365609.3365848>

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