Cryptographic Hashing in P4 Data Planes

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Motivation
Manifold P4 Applications and Programs

Imagine long list of P4 programs here
→ Few programs that require cryptographic functionality

P4 is of high interest to industry, e.g. avionics

- Rapid prototyping
- Program verification
- ...

Requires guarantees: e.g. authentication of switches

Image from https://bit.ly/2LHVmDZ
Motivation
Cryptographic Properties and Functions

Cryptographic properties commonly found in network applications and protocols

- Confidentiality
- Authenticity (data/message integrity)
- Authentication (data origin authentication)

Cryptographic functions

- Encryption
- Hash functions

→ in this work we focus on cryptographic hash functions
Motivation
Use cases for cryptographic hash functions

Data structures
- Hash maps
- Bloom-Filter

But: cryptographic functions not required
e.g. Bloom-Filter: linear-independent hashes suffice

Authenticity/Authentication
- Message Authentication Codes
- Client puzzles (TCP SYN cookies)

Cryptographic functions required
Outline

Problem Statement

Choice of Hash Function

P4 Targets and Hash Integration

Performance Results

Conclusion
Problem Statement

Feasibility of cryptographic hashing in programmable data planes

- Hash with cryptographic properties
- Hash of complete packet content
- Ideally achieving 10 GbE line-rate
- Software and hardware P4 targets
Choice of Hash Function
Cryptography vs. Performance

Cryptographic (hash) functions are
- Slow ↔ line-rate
- Complex ↔ resource consumption on target

Pseudo-cryptographic SipHash
- Optimized for small inputs
- Optimized for performance in software

Benchmarks on software system

<table>
<thead>
<tr>
<th>Hash algorithm</th>
<th>Cycles per B</th>
<th>Fixed cycles per packet</th>
<th>Cycles for 64 B</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRC32</td>
<td>0.32</td>
<td>0.00</td>
<td>10.79</td>
</tr>
<tr>
<td>Checksum</td>
<td>0.44</td>
<td>0.00</td>
<td>30.06</td>
</tr>
<tr>
<td>SipHash-2-4</td>
<td>1.06</td>
<td>56.40</td>
<td>121.10</td>
</tr>
<tr>
<td>BLAKE2b</td>
<td>3.14</td>
<td>35.85</td>
<td>232.77</td>
</tr>
<tr>
<td>HMAC-SHA256</td>
<td>5.57</td>
<td>959.69</td>
<td>1462.13</td>
</tr>
</tbody>
</table>
Available P4 Targets

...that can be extended with cryptographic hashing

- Software: t4p4s (P4ELTE), based on DPDK
- Network Processing Unit: Netronome Agilio SmartNIC (NFP-4000)
- FPGA: NetFPGA SUME (P4→NetFPGA)
- ASIC: none that we are aware of
P4 Hash Integration

t4p4s

- Trivial: link library, add extern
- Added SipHash-2-4 and HMAC-SHA512 (openssl)

NFP-4000

- Crypto security accelerator (SHA1): not available on our card
- Integrated SipHash-2-4 as extern in variation of C

NetFPGA SUME

- Externs implemented in Verilog/VHDL
- Integrated SipHash-2-4 and SHA3-512

Problem:

- Data passed between P4 program and extern is a single data word
- SDNet limit: 600 B input width
- No timing closure due to resource congestion
P4 Hash Integration

NetFPGA

Alternative P4 architecture model

Limitations

- All packets are always hashed
- Hash outcome not usable in P4
- Alternatives:
  - Hashing before P4 pipeline
  - Second P4 pipeline after hashing core
  - Traffic manager
- SHA3-512 core uses 125 MHz → clock domain crossing
Measurement Results

Setup

- Load Generator
  - CBR traffic of constant packet size
  - Precise latency measurements
- Device-under-Test (DuT)
  - Intel Xeon E5-2620 with Intel X540 NIC
  - Netronome NFP-4000 SmartNIC
  - NetFPGA SUME
- P4 program
  - L2 forwarder
  - Hashes complete packets

Disclaimer

- Open-source implementations
- Non-commercial IP cores
- Not optimized integration → proof-of-concept
- Take performance figures with grain of salt
  → conservative numbers
Measurement Results

Achievable Throughput

<table>
<thead>
<tr>
<th>Packet Size [B]</th>
<th>Throughput [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td></td>
</tr>
<tr>
<td>96</td>
<td></td>
</tr>
<tr>
<td>128</td>
<td></td>
</tr>
<tr>
<td>512</td>
<td></td>
</tr>
<tr>
<td>1024</td>
<td></td>
</tr>
<tr>
<td>1500</td>
<td></td>
</tr>
</tbody>
</table>

- t4p4s SipHash
- t4p4s HMAC SHA512
- NetFPGA SipHash
- NetFPGA SHA3-512
- NFP-4000 SipHash
### Measurement Results

#### Latency

**NetFPGA**

Stable latency: no long-tail

**t4p4s**

Typical behavior of software system/DPDK: long-tail
Measurement Results

Resource Utilization

Does the program fit on the target?

- t4p4s: trivial
- NFP-4000: no restrictions encountered
- NetFPGA:

<table>
<thead>
<tr>
<th></th>
<th>LUTs</th>
<th>Registers</th>
<th>BRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Abs.</td>
<td>%</td>
<td>Abs.</td>
</tr>
<tr>
<td>Baseline</td>
<td>64,533</td>
<td>14.90</td>
<td>109,783</td>
</tr>
<tr>
<td>SipHash-2-4</td>
<td>66,380</td>
<td>15.32</td>
<td>114,282</td>
</tr>
<tr>
<td>SHA3-512</td>
<td>73,449</td>
<td>16.95</td>
<td>118,689</td>
</tr>
</tbody>
</table>
Conclusion

The current use of hash functions in P4 programs

- Data structures might be vulnerable to attacks (hash collisions)
- Lack of programs/protocols requiring authentication and integrity
  → Cryptographic hash functions increase applicability of P4

Cryptographic hashing is target, algorithm and use-case dependent

- Line-rate possible on hardware targets
- Integration for instance by adjusting P4 architecture model
- Algorithms might be better on one target than another
  → no one-size-fits-all solution
  → P4 specification should recommend family of hash functions, including cryptographic ones