

Rapid Prototyping of Avionic Applications Using P4

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I. APPLICABILITY FOR AERONAUTICAL APPLICATIONS

The main advantage of P4 is the decorrelation between the behavior of a packet processing device and the hardware which is used. It means that engineers are not tied to a specific set of network protocols implemented by hardware vendors. This is especially relevant in the aeronautical industry where specific network protocols (e.g. ARINC standards) are used. Furthermore, devices must exclusively implement the required protocols and functionalities for safety reasons. Those two constraints prevent commodity devices to be used since they either do not support the required protocols, or implement a larger set of protocols than the ones required. With P4, the usability of commodity devices increases.

Another advantage of P4 is the simplicity and constraints put on the abstract forwarding model. Since P4 forbids dynamic memory allocation and iterations with unknown counts, formal derivations of worst-case execution time and resource usage of a P4 program are straightforward already at compile time. This is again relevant in the aeronautical industry since constraints on those cost factors are required in real-time applications.

A downside when using P4 for aeronautical applications is that egress packet scheduling cannot be directly described by P4. This limits the description of more advanced Quality-of-Service architectures envisioned for next-generation aeronautical backbones [1].

Since safety is an important aspect of aeronautical applications, specification and programming languages need to have defined behavior. While this was a problem in the 2014 specification of P4 as some aspects are incompletely specified (e.g. casting between different data types, and initial values of table entries and packet attributes) this has since been solved with P4₁₆.

Finally, time-based or time-triggered protocols cannot be directly described using P4 since there are no primitives for describing access to a clocking information, besides timestamps at ingress and egress in P4₁₆. This drawback prevents the implementation of time-synchronization protocols for packet timestamping, or egress scheduling based on time information.

II. CASE STUDY

In order to evaluate the applicability of P4 to aeronautical use-cases, we applied P4 to the case-study of Avionics Full-Duplex Switched Ethernet (AFDX), an Ethernet-based protocol for safety-critical applications standardized in ARINC 664 Part 7 [2].

An AFDX network is composed of *end-systems* and *switches* as nodes. End-systems serve as source and destination nodes in the network, over which applications send data according to bandwidth restrictions to avoid overloading. One fundamental building block of AFDX is the notion of *virtual links* (VL), which can be seen as rate-constrained network tunnels. The parameters describing a VL are: the emitter end-system of this VL, the list of receiving end-systems, static routes between emitter and receivers, the Bandwidth Allocation Gap (BAG), as well as minimum and maximum frame length. The BAG is defined as the minimum time interval between the first bit of two consecutive frames from the same VL.

III. IMPLEMENTATION OVERVIEW

AFDX switches must ensure the following functionalities for each frame entering the switch: identification of the VL; frame filtering

and policing based on VL parameters (allowed input port, BAG, and frame length limits); forwarding of the frame to the correct output ports based on the VL routing configuration.

Frames in AFDX are based on the standard Ethernet frame format. The VL identification number is encoded in the 16 least significant bits of the destination MAC address. Switch configuration and routes in P4 are saved in tables. For our case-study, we define a table containing the allowed input port of each VL and its output port. Incoming packets with invalid Virtual Link identifiers are dropped here.

Our case-study contains a simplified ingress function for AFDX with basic frame integrity checking, application of the aforementioned table, and policing. For the latter, a simple process based on validating the BAG timing properties and minimum and maximum frame sizes is described in the ARINC standard. While frame size validation is possible with P4, filtering based on the time between frames is not. Since from a functional point of view the goal is to limit the bandwidth of each VL, the standard policing mechanisms provided by P4 using meters may be used as an alternative.

Finally, the last step is to forward frames to the correct output ports. This is done using multicast by a vendor-specific mechanism.

IV. FURTHER ASPECTS

Our implementation is based on P4₁₄ as by the time of implementation more hardware supported this P4 version. We listed here only a subset of the functionalities needed by an AFDX switch. More advanced features such as operational modes and monitoring functionalities based on SNMP can also be implemented using P4. We performed a performance analysis regarding throughput, latency and profiling for three P4 targets: An Intel DPDK-based software switch, a Netronome Agilio CX SmartNIC network processor platform, and a prototype FPGA-based platform.

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